**I. COURSE TITLE:** Computer Architecture and Design

**COURSE NUMBER:** 2254 **COURSE PREFIX:** EENG

**II. PREREQUISITES:** CSCI 1140 & 1141 or permission of instructor

**III. CREDIT HOURS:** 4 **LECTURE HOURS:** 3

**LABORATORY HOURS:** 1 (2 contact) **OBSERVATION HOURS:** 0

**IV. COURSE DESCRIPTION:**

This is an introductory course into computer architecture. This class will assemble a single board computer with a lecture section before each section to describe how the section works. Use of Oscilloscope, Digital Logic probe and Millimeter are used to make measurements and troubleshoot each section.

**V. ADOPTED TEXT(S):**

Micro-Processor Trainer Model 809 (Supplied with Lab computer)

**VI. LEARNING OBJECTIVES:**

1. Microprocessor Architecture
2. Assembly Language programming
3. Bus Timing Diagrams
4. Bus Structures
5. Memory Technologies and Interfacing
6. Input/output interface
7. Interrupt-processed input/output
8. Direct memory access(DMA)
9. Microcontroller applications
10. Microprocessor- Based Communications

**VII. COURSE METHODOLOGY**

Classes will consist of lectures, class discussions, small group projects, videos, outside assignments and supplemental materials. Interactive class discussion is encouraged and staying current on reading assignments necessary to be able to actively participate in class discussions.

**VIII. GRADING:**

Grading will follow the policy in the SSCC catalog.

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **90** | **–** | **100** |
| **B** | **80** | **–** | **89** |
| **C** | **70** | **–** | **79** |
| **D** | **60** | **–** | **69** |
| **F** | **0** | **–** | **59** |

**IX COURSE OUTLINE/CALENDER:**

**Sample Weekly Schedule:**

Week 1 Digital Logic Fundamentals Hand Outs

Binary numbers Test 1

Week 2 Power supply Circuitry Section 1.3

Week 3 DMA, Binary Counters Section 1.4

Test 2

Week 4 Ram Memory Section 1.5

Week 5 Ram Battery Backup Section 1.6

Week 6 8085A internal structure & Section 1.7

Operation

Week 7 Operating in the Binary Mode Section 2& 2.2

DMA/Run, MVI,IN,OUT,JMP,HLT Test 3

Week 8 Parallel input/output ports Sections 3.1-3.3 Addressing, timing, Rd, Wr cycle

Week 9 Parallel Output Ports & Display Sections 3.4-3.5

Seven segments

Week 10 Software Sections 4.1- 4.5

Week 11 Monitoring system Rom,8255, Sections 5.1-5.5

Keyboard, ,address Display

Week 12 Operating in Hex Mode Sections 6.1-6.3

Flags, Debug mode Test 5

Week 13 Programming Sections 7.1-7.4

Week 14 Serial Communications Sections 8.1-8.2

Week 15 Operating in the Mneumonic Sections 9.1-9.2

Mode

Week 16 **Final**

**X. OTHER REQUIRED BOOKS AND MATERIALS:**

Lab fees $75.00 to cover microprocessor and other tools

**XI. EVALUATION:**

Instructor will specify which criteria apply to a particular assignment.

Students will complete multiple exercises using the appropriate hardware and software. Other assignments, projects and exercises may be assigned and graded at the discretion of the instructor.

**XII. SPECIFIC MANAGEMENT REQUIREMENTS:**

None

**XIII. OTHER INFORMATION:**

**FERPA:** Students need to understand that your work may be seen by others. Others may see your work when being distributed, during group project work, or if it is chosen for demonstration purposes.

Students also need to know that there is a strong possibility that your work may be submitted to other entities for the purpose of plagiarism checks.

**DISABILITIES:** Students with disabilities may contact the Disabilities Service Office, Central Campus, at 800-628-7722 or 937-393-3431.